**CHAPTER 1**

1. Computer technology is changing at a \_\_\_\_\_\_\_\_\_\_ pace.  
   a. slow  
   b. slow to medium  
   c. rapid  
   d. non-existent
2. Computer \_\_\_\_\_\_\_\_\_ refers to those attributes that have a direct impact on the logical execution of a program.  
   a. organization  
   b. specifics  
   c. design  
   d. architecture
3. Architectural attributes include \_\_\_\_\_\_\_\_\_\_ .  
   a. I/O mechanisms  
   b. control signals  
   c. interfaces  
   d. memory technology used
4. \_\_\_\_\_\_\_\_\_ attributes include hardware details transparent to the programmer.  
   a. Interface  
   b. Organizational  
   c. Memory  
   d. Architectural
5. It is a(n) \_\_\_\_\_\_\_\_\_ design issue whether a computer will have a multiply instruction.  
   a. architectural  
   b. memory  
   c. elementary  
   d. organizational
6. It is a(n) \_\_\_\_\_\_\_\_\_ issue whether the multiply instruction will be implemented by a special multiply unit or by a mechanism that makes repeated use of the add unit of the system.  
     
   a. architectural  
   b. memory  
   c. mechanical  
   d. organizational
7. A \_\_\_\_\_\_\_\_\_\_ system is a set of interrelated subsystems.  
   a. secondary  
   b. hierarchical  
   c. complex  
   d. functional
8. An I/O device is referred to as a \_\_\_\_\_\_\_\_\_\_.  
   a. CPU  
   b. control device  
   c. peripheral  
   d. register
9. When data are moved over longer distances, to or from a remote device, the process is known as \_\_\_\_\_\_\_\_\_\_.  
   a. data communications  
   b. registering  
   c. structuring  
   d. data transport
10. The \_\_\_\_\_\_\_\_\_ stores data.  
    a. system bus  
    b. I/O  
    c. main memory  
    d. control unit
11. A common example of system interconnection is by means of a \_\_\_\_\_\_\_\_\_\_.  
    a. register  
    b. system bus  
    c. data transport  
    d. control device
12. The \_\_\_\_\_\_\_\_\_\_ moves data between the computer and its external environment.  
    a. data transport  
    b. I/O  
    c. register  
    d. CPU interconnection
13. A \_\_\_\_\_\_\_\_\_ is a mechanism that provides for communication among CPU, main memory, and I/O.  
    a. system interconnection  
    b. CPU interconnection  
    c. peripheral  
    d. processor
14. \_\_\_\_\_\_\_\_\_ provide storage internal to the CPU.  
      
    a. Control units  
    b. ALUs  
    c. Main memory  
    d. Registers
15. The \_\_\_\_\_\_\_\_\_\_ performs the computer's data processing functions.  
    a. Register  
    b. CPU interconnection  
    c. ALU  
    d. system bus
16. There is a tremendous variety of products, from single-chip microcomputers costing a few dollars to supercomputers costing tens of millions of dollars that can rightly claim the name "computer".  
    a. True  
    b. False
17. The variety of computer products is exhibited only in cost.  
    a. True  
    b. False
18. Computer organization refers to attributes of a system visible to the programmer.  
    a. True  
    b. False
19. Changes in computer technology are finally slowing down.  
    a. True  
    b. False
20. The number of bits used to represent various data types is an example of an architectural attribute.  
    a. True  
    b. False
21. Interfaces between the computer and peripherals is an example of an organizational attribute.  
    a. True  
    b. False
22. Historically the distinction between architecture and organization has not been an important one.  
    a. True  
    b. False
23. A particular architecture may span many years and encompass a number of different computer models, its organization changing with changing technology.  
    a. True  
    b. False
24. A microcomputer architecture and organization relationship is not very close.  
    a. True  
    b. False
25. Changes in technology not only influence organization but also result in the introduction of more powerful and more complex architectures.  
    a. True  
    b. False
26. The hierarchical nature of complex systems is essential to both their design and their description.  
    a. True  
    b. False
27. Both the structure and functioning of a computer are, in essence, simple.  
    a. True  
    b. False
28. A computer must be able to process, store, move, and control data.  
    a. True  
    b. False
29. When data are moved over longer distances, to or from a remote device, the process is known as data transport.  
    a. True  
    b. False (data communication)
30. The textbook for this course is about the structure and function of computers.  
    a. True  
    b. False

**CHAPTER 2**

1. The \_\_\_\_\_\_\_\_\_ was the world's first general-purpose electronic digital computer.  
   a. UNIVAC  
   b. MARK IV  
   c. ENIAC  
   d. Hollerith's Counting Machine
2. The Electronic Numerical Integrator and Computer project was a response to U.S. needs during \_\_\_\_\_\_\_\_\_.  
   a. the Civil War  
   b. the French-American War  
   c. World War I  
   d. World War II
3. The ENIAC used \_\_\_\_\_\_\_\_\_\_.  
   a. vacuum tubes  
   b. integrated circuits  
   c. IAS

d. transistors

1. The ENIAC is an example of a \_\_\_\_\_\_\_\_\_ generation computer.  
   a. first  
   b. second  
   c. third  
   d. fourth
2. The \_\_\_\_\_\_\_\_\_\_ interprets the instructions in memory and causes them to be executed.  
   a. main memory  
   b. control unit  
   c. I/O  
   d. arithmetic and logic unit
3. The memory of the IAS consists of 1000 storage locations called \_\_\_\_\_\_\_\_\_\_.  
   a. opcodes  
   b. wafers  
   c. VLSIs  
   d. words (each 40 bits)
4. The \_\_\_\_\_\_\_\_\_\_ contains the 8-bit opcode instruction being executed.  
   a. memory buffer register  
   b. instruction buffer register  
   c. instruction register  
   d. memory address register
5. During the \_\_\_\_\_\_\_\_\_ the opcode of the next instruction is loaded into the IR and the address portion is loaded into the MAR.  
   a. execute cycle  
   b. fetch cycle  
   c. instruction cycle  
   d. clock cycle
6. Second generation computers used \_\_\_\_\_\_\_\_\_\_.  
   a. integrated circuits  
   b. Transistors  
   c. vacuum tubes  
   d. large-scale integration
7. The \_\_\_\_\_\_\_\_\_\_ defines the third generation of computers.  
   a. integrated circuit  
   b. vacuum tube  
   c. transistor  
   d. VLSI
8. The use of multiple processors on the same chip is referred to as \_\_\_\_\_\_\_\_\_\_ and provides the potential to increase performance without increasing the clock rate.  
   a. multicore  
   b. GPU  
   c. data channels  
   d. MPC
9. With the \_\_\_\_\_\_\_\_\_\_, Intel introduced the use of superscalar techniques that allow multiple instructions to execute in parallel.  
   a. Core  
   b. 8080  
   c. 80486  
   d. Pentium
10. The \_\_\_\_\_\_\_\_\_\_ measures the ability of a computer to complete a single task.  
    a. clock speed  
    b. speed metric  
    c. execute cycle  
    d. cycle time
11. ARM processors are designed to meet the needs of \_\_\_\_\_\_\_\_\_.  
    a. embedded real-time systems  
    b. application platforms  
    c. secure applications  
    d. all of the above
12. One increment, or pulse, of the system clock is referred to as a \_\_\_\_\_\_\_\_\_.  
    a. clock tick  
    b. cycle time  
    c. clock rate  
    d. cycle speed
13. The IAS is the prototype of all subsequent general-purpose computers.  
    a. True  
    b. False
14. The IAS operates by repetitively performing an instruction cycle.  
    a. True  
    b. False
15. Computers are classified into generations based on the fundamental hardware technology employed.  
    a. True  
    b. False
16. IBM's System/360 was the industry's first planned family of computers.  
    a. True  
    b. False
17. A common measure of performance for a processor is the rate at which instructions are executed, expressed as billions of instructions per seconds (BIPS).  
    a. True  
    b. False
18. John Mauchly and John Eckert designed the ENIAC.  
    a. True  
    b. False
19. The world's first general-purpose electronic digital computer was designed and constructed at The Ohio State University.  
    a. True  
    b. False
20. The major drawback of the EDVAC was that it had to be programmed manually by setting switches and plugging and unplugging cables.  
    a. True  
    b. False
21. Backward compatible means that the programs written for the older machines can be executed on the new machine.  
    a. True  
    b. False
22. A vacuum tube is a solid-state device made from silicon.  
    a. True  
    b. False
23. System software was introduced in the third generation of computers.  
    a. True  
    b. False (2nd)
24. A wafer is made of silicon and is broken up into chips which consists of many gates and/or memory cells plus a number of input and output attachment points.  
    a. True  
    b. False
25. Intel's 4004 was the first chip to contain all of the components of a CPU on a single chip.  
    a. True  
    b. False
26. Designers wrestle with the challenge of balancing processor performance with that of main memory and other computer components.  
    a. True  
    b. False
27. The Intel x86 evolved from RISC design principles and is used in embedded systems.  
    a. True  
    b. False (CISC)

**CHAPTER 3**

1. Virtually all contemporary computer designs are based on concepts developed by \_\_\_\_\_\_\_\_\_\_ at the Institute for Advanced Studies, Princeton.  
   a. John Maulchy  
   b. John von Neumann  
   c. Herman Hollerith  
   d. John Eckert
2. The von Neumann architecture is based on which concept?  
   a. data and instructions are stored in a single read-write memory  
   b. the contents of this memory are addressable by location  
   c. execution occurs in a sequential fashion  
   d. all of the above
3. A sequence of codes or instructions is called \_\_\_\_\_\_\_\_\_\_.  
   a. software  
   b. memory  
   c. an interconnect  
   d. a register
4. The processing required for a single instruction is called a(n) \_\_\_\_\_\_\_\_\_\_ cycle.  
   a. execute  
   b. fetch  
   c. instruction  
   d. packet
5. A(n) \_\_\_\_\_\_\_\_\_ is generated by a failure such as power failure or memory parity error.  
   a. I/O interrupt  
   b. hardware failure interrupt  
   c. timer interrupt  
   d. program interrupt
6. A(n) \_\_\_\_\_\_\_\_\_ is generated by some condition that occurs as a result of an instruction execution.  
   a. timer interrupt  
   b. I/O interrupt  
   c. program interrupt  
   d. hardware failure interrupt
7. The interconnection structure must support which transfer?  
   a. memory to processor  
   b. processor to memory  
   c. I/O to or from memory  
   d. all of the above
8. A bus that connects major computer components (processor, memory, I/O) is called a \_\_\_\_\_\_\_\_\_\_.  
   a. system bus  
   b. address bus  
   c. data bus  
   d. control bus
9. The \_\_\_\_\_\_\_\_\_\_ are used to designate the source or destination of the data on the data bus.  
   a. system lines  
   b. data lines  
   c. control lines  
   d. address lines
10. The data lines provide a path for moving data among system modules and are collectively called the \_\_\_\_\_\_\_\_\_.  
    a. control bus  
    b. address bus  
    c. data bus  
    d. system bus
11. A \_\_\_\_\_\_\_\_\_\_ is the high-level set of rules for exchanging packets of data between devices.  
    a. bus  
    b. protocol  
    c. packet  
    d. QPI
12. Each data path consists of a pair of wires (referred to as a \_\_\_\_\_\_\_\_\_\_) that transmits data one bit at a time.  
    a. lane  
    b. path  
    c. line  
    d. bus
13. The \_\_\_\_\_\_\_\_\_ receives read and write requests from the software above the TL and creates request packets for transmission to a destination via the link layer.  
    a. transaction layer  
    b. root layer  
    c. configuration layer  
    d. transport layer
14. The TL supports which of the following address spaces?  
    a. memory  
    b. I/O  
    c. message  
    d. all of the above
15. The QPI \_\_\_\_\_\_\_\_\_ layer is used to determine the course that a packet will traverse across the available system interconnects.  
    a. link  
    b. protocol  
    c. routing  
    d. physical
16. At a top level, a computer consists of CPU, memory, and I/O components. TRUE
17. The basic function of a computer is to execute programs. TRUE
18. Program execution consists of repeating the process of instruction fetch and instruction execution. TRUE
19. Interrupts do not improve processing efficiency. FALSE
20. An I/O module cannot exchange data directly with the processor. FALSE
21. A key characteristic of a bus is that it is not a shared transmission medium. FALSE
22. Computer systems contain a number of different buses that provide pathways between components at various levels of the computer system hierarchy. TRUE
23. In general, the more devices attached to the bus, the greater the bus length and hence the greater the propagation delay. TRUE
24. It is not possible to connect I/O controllers directly onto the system bus. FALSE
25. The method of using the same lines for multiple purposes is known as time multiplexing. TRUE
26. Timing refers to the way in which events are coordinated on the bus. TRUE
27. With asynchronous timing the occurrence of events on the bus is determined by a clock. FALSE
28. Because all devices on a synchronous bus are tied to a fixed clock rate, the system cannot take advantage of advances in device performance. TRUE
29. The unit of transfer at the link layer is a phit and the unit transfer at the physical layer is a flit. FALSE
30. A key requirement for PCIe is high capacity to support the needs of higher data rate I/O devices such as Gigabit Ethernet. TRUE

**CHAPTER 4**

1. \_\_\_\_\_\_\_\_\_\_ refers to whether memory is internal or external to the computer.  
   a. Location  
   b. Access  
   c. Hierarchy  
   d. Tag
2. Internal memory capacity is typically expressed in terms of \_\_\_\_\_\_\_\_\_.  
   a. hertz  
   b. nanos  
   c. bytes  
   d. LOR
3. For internal memory, the \_\_\_\_\_\_\_\_\_\_ is equal to the number of electrical lines into and out of the memory module.  
   a. access time  
   b. unit of transfer  
   c. capacity  
   d. memory ratio
4. "Memory is organized into records and access must be made in a specific linear sequence" is a description of \_\_\_\_\_\_\_\_\_\_.  
   a. sequential access  
   b. direct access  
   c. random access  
   d. associative
5. Individual blocks or records have a unique address based on physical location with \_\_\_\_\_\_\_\_\_\_.  
   a. associative  
   b. physical access  
   c. direct access  
   d. sequential access
6. For random-access memory, \_\_\_\_\_\_\_\_\_\_ is the time from the instant that an address is presented to the memory to the instant that data have been stored or made available for use.  
   a. memory cycle time  
   b. direct access  
   c. transfer rate  
   d. access time
7. The \_\_\_\_\_\_\_\_ consists of the access time plus any additional time required before a second access can commence.  
     
   a. latency  
   b. memory cycle time  
   c. direct access  
   d. transfer rate
8. A portion of main memory used as a buffer to hold data temporarily that is to be read out to disk is referred to as a \_\_\_\_\_\_\_\_\_.  
   a. disk cache  
   b. latency  
   c. virtual address  
   d. miss
9. A line includes a \_\_\_\_\_\_\_\_\_ that identifies which particular block is currently being stored.  
   a. cache  
   b. hit  
   c. tag  
   d. locality
10. \_\_\_\_\_\_\_\_\_\_ is the simplest mapping technique and maps each block of main memory into only one possible cache line.  
    a. Direct mapping  
    b. Associative mapping  
    c. Set associative mapping  
    d. None of the above
11. When using the \_\_\_\_\_\_\_\_\_\_ technique all write operations made to main memory are made to the cache as well.  
    a. write back  
    b. LRU  
    c. write through  
    d. unified cache
12. The key advantage of the \_\_\_\_\_\_\_\_\_\_ design is that it eliminates contention for the cache between the instruction fetch/decode unit and the execution unit.  
    a. logical cache  
    b. split cache  
    c. unified cache  
    d. physical cache
13. The Pentium 4 \_\_\_\_\_\_\_\_\_ component executes micro-operations, fetching the required data from the L1 data cache and temporarily storing results in registers.  
    a. fetch/decode unit  
    b. out-of-order execution logic  
    c. execution unit  
    d. memory subsystem
14. In reference to access time to a two-level memory, a \_\_\_\_\_\_\_\_\_ occurs if an accessed word is not found in the faster memory.  
    a. miss  
    b. hit  
    c. line  
    d. tag
15. A logical cache stores data using \_\_\_\_\_\_\_\_\_\_.  
    a. physical addresses  
    b. virtual addresses  
    c. random addresses  
    d. none of the above
16. No single technology is optimal in satisfying the memory requirements for a computer system. TRUE
17. A typical computer system is equipped with a hierarchy of memory subsystems, some internal to the system and some external. TRUE
18. External memory is often equated with main memory. FALSE
19. The processor requires its own local memory. TRUE
20. Cache is not a form of internal memory. FALSE
21. The unit of transfer must equal a word or an addressable unit. FALSE
22. Both sequential access and direct access involve a shared read-write mechanism. TRUE
23. In a volatile memory, information decays naturally or is lost when electrical power is switched off. TRUE
24. To achieve greatest performance the memory must be able to keep up with the processor. TRUE
25. Secondary memory is used to store program and data files and is usually visible to the programmer only in terms of individual bytes or words. FALSE
26. The L1 cache is slower than the L3 cache. FALSE
27. With write back updates are made only in the cache.TRUE
28. It has become possible to have a cache on the same chip as the processor.TRUE
29. All of the Pentium processors include two on-chip L1 caches, one for data and one for instructions. TRUE
30. Cache design for HPC is the same as that for other hardware platforms and applications. FALSE

**CHAPTER 5**

1. Which properties do all semiconductor memory cells share?  
   a. they exhibit two stable states which can be used to represent binary 1 and 0  
   b. they are capable of being written into to set the state  
   c. they are capable of being read to sense the state  
   d. all of the above
2. One distinguishing characteristic of memory that is designated as \_\_\_\_\_\_\_\_\_ is that it is possible to both to read data from the memory and to write new data into the memory easily and rapidly.  
   a. RAM  
   b. ROM  
   c. EPROM  
   d. EEPROM
3. Which of the following memory types are nonvolatile?  
   a. erasable PROM  
   b. programmable ROM  
   c. flash memory  
   d. all of the above
4. In a \_\_\_\_\_\_\_\_\_, binary values are stored using traditional flip-flop logic-gate configurations.  
   a. ROM  
   b. SRAM  
   c. DRAM  
   d. RAM
5. A \_\_\_\_\_\_\_\_\_\_ contains a permanent pattern of data that cannot be changed, is nonvolatile, and cannot have new data written into it.  
   a. RAM  
   b. SRAM  
   c. ROM  
   d. flash memory
6. With \_\_\_\_\_\_\_\_\_ the microchip is organized so that a section of memory cells are erased in a single action.  
   a. flash memory  
   b. SDRAM  
   c. DRAM  
   d. EEPROM
7. \_\_\_\_\_\_\_\_\_\_ can be caused by harsh environmental abuse, manufacturing defects, and wear.  
     
   a. SEC errors  
   b. Hard errors  
   c. Syndrome errors  
   d. Soft errors
8. \_\_\_\_\_\_\_\_\_ can be caused by power supply problems or alpha particles.  
   a. Soft errors  
   b. AGT errors  
   c. Hard errors  
   d. SEC errors
9. The \_\_\_\_\_\_\_\_\_ exchanges data with the processor synchronized to an external clock signal and running at the full speed of the processor/memory bus without imposing wait states.  
   a. DDR-DRAM  
   b. SDRAM  
   c. CDRAM  
   d. none of the above
10. \_\_\_\_\_\_\_ can send data to the processor twice per clock cycle.  
    a. CDRAM  
    b. SDRAM  
    c. DDR-DRAM  
    d. RDRAM
11. \_\_\_\_\_\_\_\_\_\_ increases the data transfer rate by increasing the operational frequency of the RAM chip and by increasing the prefetch buffer from 2 bits to 4 bits per chip.  
    a. DDR2  
    b. RDRAM  
    c. CDRAM  
    d. DDR3
12. \_\_\_\_\_\_\_\_ increases the prefetch buffer size to 8 bits.  
    a. CDRAM  
    b. RDRAM  
    c. DDR3  
    d. all of the above
13. Theoretically, a DDR module can transfer data at a clock rate in the range of \_\_\_\_\_\_\_\_\_\_ MHz.  
    a. 200 to 600  
    b. 400 to 1066  
    c. 600 to 1400  
    d. 800 to 1600
14. A DDR3 module transfers data at a clock rate of \_\_\_\_\_\_\_\_\_\_ MHz.  
    a. 600 to 1200  
    b. 800 to 1600  
    c. 1000 to 2000  
    d. 1500 to 3000
15. The \_\_\_\_\_\_\_\_ enables the RAM chip to preposition bits to be placed on the data bus as rapidly as possible.  
    a. flash memory  
    b. Hamming code  
    c. RamBus  
    d. buffer
16. The basic element of a semiconductor memory is the memory cell.TRUE
17. A characteristic of ROM is that it is volatile.FALSE
18. RAM must be provided with a constant power supply.TRUE
19. The two traditional forms of RAM used in computers are DRAM and SRAM.TRUE
20. A static RAM will hold its data as long as power is supplied to it.TRUE
21. Nonvolatile means that power must be continuously supplied to the memory to preserve the bit values.FALSE
22. The advantage of RAM is that the data or program is permanently in main memory and need never be loaded from a secondary storage device.FALSE
23. Semiconductor memory comes in packaged chips.TRUE
24. All DRAMs require a refresh operation.TRUE
25. An error-correcting code enhances the reliability of the memory at the cost of added complexity.TRUE
26. DRAM is much costlier than SRAM. FALSE
27. RDRAM is limited by the fact that it can only send data to the processor once per bus clock cycle.FALSE
28. The prefetch buffer is a memory cache located on the RAM chip. TRUE
29. The SRAM on the CDRAM cannot be used as a buffer to support the serial access of a block of data.FALSE
30. A number of chips can be grouped together to form a memory bank.TRUE

**CHAPTER 6**

1. Greater ability to withstand shock and damage, improvement in the uniformity of the magnet film surface to increase disk reliability, and a significant reduction in overall surface defects to help reduce read-write errors, are all benefits of \_\_\_\_\_\_\_\_\_\_\_.  
   a. magnetic read and write mechanisms  
   b. platters  
   c. the glass substrate  
   d. a solid state drive
2. Adjacent tracks are separated by \_\_\_\_\_\_\_\_\_.  
   a. sectors  
   b. gaps  
   c. pits  
   d. heads
3. Data are transferred to and from the disk in \_\_\_\_\_\_\_\_\_\_.

a. tracks

b. gaps

c. sectors

d. pits

1. In most contemporary systems fixed-length sectors are used, with \_\_\_\_\_\_\_\_\_ bytes being the nearly universal sector size.  
   a. 64  
   b. 128  
   c. 256  
   d. 512
2. Scanning information at the same rate by rotating the disk at a fixed speed is known as the \_\_\_\_\_\_\_\_\_.  
   a. constant angular velocity  
   b. magnetoresistive  
   c. rotational delay  
   d. constant linear velocity
3. The disadvantage of \_\_\_\_\_\_\_\_\_ is that the amount of data that can be stored on the long outer tracks is only the same as what can be stored on the short inner tracks.  
   a. SSD  
   b. CAV (constant angular velocity)  
   c. ROM  
   d. CLV
4. A \_\_\_\_\_\_\_\_\_\_ disk is permanently mounted in the disk drive, such as the hard disk in a personal computer.  
   a. nonremovable  
   b. movable-head  
   c. double sided  
   d. removable
5. When the magnetizable coating is applied to both sides of the platter the disk is then referred to as \_\_\_\_\_\_\_\_\_.  
   a. multiple sided  
   b. substrate  
   c. double sided  
   d. all of the above
6. The set of all the tracks in the same relative position on the platter is referred to as a \_\_\_\_\_\_\_\_\_.  
   a. floppy disk  
   b. single-sided disk  
   c. sector  
   d. cylinder
7. The sum of the seek time and the rotational delay equals the \_\_\_\_\_\_\_\_\_, which is the time it takes to get into position to read or write.  
   a. access time  
   b. gap time  
   c. transfer time  
   d. constant angular velocity
8. \_\_\_\_\_\_\_\_\_\_ is the standardized scheme for multiple-disk database design.  
   a. RAID  
   b. CAV  
   c. CLV  
   d. SSD
9. RAID level \_\_\_\_\_\_\_\_ has the highest disk overhead of all RAID types.  
   a. 0  
   b. 1  
   c. 3  
   d. 5
10. A \_\_\_\_\_\_\_\_\_ is a high-definition video disk that can store 25 Gbytes on a single layer on a single side.  
    a. DVD  
    b. DVD-R  
    c. DVD-RW  
    d. Blu-ray DVD
11. \_\_\_\_\_\_\_\_ is when the disk rotates more slowly for accesses near the outer edge than for those near the center.  
    a. Constant angular velocity (CAV)  
    b. Magnetoresistive  
    c. Constant linear velocity (CLV)  
    d. Seek time
12. The areas between pits are called \_\_\_\_\_\_\_\_\_.  
    a. lands  
    b. sectors  
    c. cylinders  
    d. strips
13. Magnetic disks are the foundation of external memory on virtually all computer systems.TRUE
14. During a read or write operation, the head rotates while the platter beneath it stays stationary.FALSE
15. The width of a track is double that of the head.FALSE
16. There are typically hundreds of sectors per track and they may be either fixed or variable lengths.TRUE
17. A bit near the center of a rotating disk travels past a fixed point slower than a bit on the outside.TRUE
18. The disadvantage of using CAV is that individual blocks of data can only be directly addressed by track and sector.FALSE
19. A removable disk can be removed and replaced with another disk.TRUE
20. The head must generate or sense an electromagnetic field of sufficient magnitude to write and read properly. TRUE
21. The transfer time to or from the disk does not depend on the rotation speed of the disk.FALSE
22. RAID is a set of physical disk drives viewed by the operating system as a single logical drive.TRUE
23. RAID level 0 is not a true member of the RAID family because it does not include redundancy to improve performance.TRUE
24. Because data are striped in very small strips, RAID 3 cannot achieve very high data transfer rates.FALSE
25. The SSDs now on the market use a type of semiconductor memory referred to as flash memory.TRUE
26. SSD performance has a tendency to speed up as the device is used.FALSE
27. Flash memory becomes unusable after a certain number of writes.TRUE

**CHAPTER 7**

1. The \_\_\_\_\_\_\_\_\_ contains logic for performing a communication function between the peripheral and the bus.  
   a. I/O channel  
   b. I/O module  
   c. I/O processor  
   d. I/O command
2. The most common means of computer/user interaction is a \_\_\_\_\_\_\_\_\_\_.  
   a. keyboard/monitor  
   b. mouse/printer  
   c. modem/printer  
   d. monitor/printer
3. The I/O function includes a \_\_\_\_\_\_\_\_\_ requirement to coordinate the flow of traffic between internal resources and external devices.  
   a. cycle  
   b. status reporting  
   c. control and timing  
   d. data
4. An I/O module that takes on most of the detailed processing burden, presenting a high-level interface to the processor, is usually referred to as an \_\_\_\_\_\_\_\_\_.  
   a. I/O channel  
   b. I/O command  
   c. I/O controller  
   d. device controller
5. An I/O module that is quite primitive and requires detailed control is usually referred to as an \_\_\_\_\_\_\_\_\_.  
   a. I/O command  
   b. I/O controller  
   c. I/O channel  
   d. I/O processor
6. The \_\_\_\_\_\_\_\_\_ command causes the I/O module to take an item of data from the data bus and subsequently transmit that data item to the peripheral.  
   a. control  
   b. test  
   c. read  
   d. write
7. The \_\_\_\_\_\_\_\_ command is used to activate a peripheral and tell it what to do.  
     
   a. control  
   b. test  
   c. read  
   d. write
8. \_\_\_\_\_\_\_\_ is when the DMA module must force the processor to suspend operation temporarily.  
   a. Interrupt  
   b. Thunderbolt  
   c. Cycle stealing  
   d. Lock down
9. The 8237 DMA is known as a \_\_\_\_\_\_\_\_\_ DMA controller.  
   a. command  
   b. cycle stealing  
   c. interrupt  
   d. fly-by
10. \_\_\_\_\_\_\_ is a digital display interface standard now widely adopted for computer monitors, laptop displays, and other graphics and video interfaces.  
    a. DisplayPort  
    b. PCI Express  
    c. Thunderbolt  
    d. InfiniBand
11. The \_\_\_\_\_\_\_\_ layer is the key to the operation of Thunderbolt and what makes it attractive as a high-speed peripheral I/O technology.  
    a. cable  
    b. application  
    c. common transport  
    d. physical
12. The Thunderbolt protocol \_\_\_\_\_\_\_\_\_ layer is responsible for link maintenance including hot-plug detection and data encoding to provide highly efficient data transfer.  
    a. cable  
    b. application  
    c. common transport  
    d. physical
13. The \_\_\_\_\_\_\_\_ contains I/O protocols that are mapped on to the transport layer.  
    a. cable  
    b. application  
    c. common transport  
    d. physical
14. A \_\_\_\_\_\_\_\_ is used to connect storage systems, routers, and other peripheral devices to an InfiniBand switch.  
    a. target channel adapter  
    b. InfiniBand switch  
    c. host channel adapter  
    d. subnet
15. A \_\_\_\_\_\_\_\_ connects InfiniBand subnets, or connects an InfiniBand switch to a network such as a local area network, wide area network, or storage area network.  
    a. memory controller  
    b. TCA  
    c. HCA  
    d. router
16. A set of I/O modules is a key element of a computer system.TRUE
17. An I/O module must recognize one unique address for each peripheral it controls.TRUE
18. I/O channels are commonly seen on microcomputers, whereas I/O controllers are used on mainframes.FALSE
19. It is the responsibility of the processor to periodically check the status of the I/O module until it finds that the operation is complete.TRUE
20. With isolated I/O there is a single address space for memory locations and I/O devices.FALSE
21. A disadvantage of memory-mapped I/O is that valuable memory address space is used up. TRUE
22. The disadvantage of the software poll is that it is time consuming.TRUE
23. With a daisy chain the processor just picks the interrupt line with the highest priority.FALSE
24. Bus arbitration makes use of vectored interrupts.TRUE
25. The rotating interrupt mode allows the processor to inhibit interrupts from certain devices. FALSE
26. Because the 82C55A is programmable via the control register, it can be used to control a variety of simple peripheral devices.TRUE
27. When large volumes of data are to be moved, a more efficient technique is direct memory access (DMA).TRUE
28. An I/O channel has the ability to execute I/O instructions, which gives it complete control over I/O operations.TRUE
29. A multipoint external interface provides a dedicated line between the I/O module and the external device.FALSE
30. A Thunderbolt compatible peripheral interface is no more complex than that of a simple USB device.FALSE

**CHAPTER 8**

1. The \_\_\_\_\_\_\_\_\_\_ is a program that controls the execution of application programs and acts as an interface between applications and the computer hardware.  
   a. job control language  
   b. operating system  
   c. batch system  
   d. nucleus
2. Facilities and services provided by the OS that assist the programmer in creating programs are in the form of \_\_\_\_\_\_\_\_\_ programs that are not actually part of the OS but are accessible through the OS.  
   a. utility  
   b. multitasking  
   c. JCL  
   d. logical address
3. The \_\_\_\_\_\_\_\_\_ defines the repertoire of machine language instructions that a computer can follow.  
   a. ABI  
   b. API  
   c. HLL  
   d. ISA
4. The \_\_\_\_\_\_\_\_\_ defines the system call interface to the operating system and the hardware resources and services available in a system through the user instruction set architecture.  
   a. HLL  
   b. API  
   c. ABI  
   d. ISA
5. The \_\_\_\_\_\_\_\_ gives a program access to the hardware resources and services available in a system through the user instruction set architecture supplemented with high-level language library calls.  
   a. JCL  
   b. ISA  
   c. ABI  
   d. API
6. A \_\_\_\_\_\_\_\_\_ system works only one program at a time.  
   a. batch  
   b. uniprogramming  
   c. kernel  
   d. privileged instruction
7. A \_\_\_\_\_\_\_\_\_ is a special type of programming language used to provide instructions to the monitor.  
   a. job control language  
   b. multiprogram  
   c. kernel  
   d. utility
8. The \_\_\_\_\_\_\_\_ scheduler is also known as the dispatcher.  
   a. long-term  
   b. medium-term  
   c. short-term  
   d. I/O
9. A \_\_\_\_\_\_\_\_\_ is an actual location in main memory.  
   a. logical address  
   b. partition address  
   c. base address  
   d. physical address
10. \_\_\_\_\_\_\_\_ is when the processor spends most of its time swapping pages rather than executing instructions.  
    a. Swapping  
    b. Thrashing  
    c. Paging  
    d. Multitasking
11. Virtual memory schemes make use of a special cache called a \_\_\_\_\_\_\_\_ for page table entries.  
    a. TLB  
    b. HLL  
    c. VMC  
    d. SPB
12. With \_\_\_\_\_\_\_\_\_ the virtual address is the same as the physical address.  
    a. unsegmented unpaged memory  
    b. unsegmented paged memory  
    c. segmented unpaged memory  
    d. segmented paged memory
13. A \_\_\_\_\_\_\_\_\_ is a collection of memory regions.  
    a. APX  
    b. nucleus  
    c. domain  
    d. page table
14. The OS maintains a \_\_\_\_\_\_\_\_\_\_ for each process that shows the frame location for each page of the process.  
    a. kernel  
    b. page table  
    c. TLB  
    d. logical address
15. The \_\_\_\_\_\_\_\_\_ scheduler determines which programs are admitted to the system for processing.  
    a. long-term  
    b. medium-term  
    c. short-term  
    d. I/O
16. Scheduling and memory management are the two OS functions that are most relevant to the study of computer organization and architecture.TRUE
17. The end user is concerned mainly with the computer's architecture.FALSE
18. The most important system program is the OS.TRUE
19. The ABI is the boundary between hardware and software.FALSE
20. The OS must determine how much processor time is to be devoted to the execution of a particular user program.TRUE
21. With a batch operating system the user does not have direct access to the processor.TRUE
22. Privileged instructions are certain instructions that are designated special and can be executed only by the monitor.TRUE
23. Uniprogramming is the central theme of modern operating systems.FALSE
24. Both batch multiprogramming and time sharing use multiprogramming.TRUE
25. An interrupt is a hardware-generated signal to the processor.TRUE
26. Swapping is an I/O operation.TRUE
27. With demand paging it is necessary to load an entire process into main memory.FALSE
28. The Pentium II includes hardware for both segmentation and paging.TRUE
29. ARM provides a versatile virtual memory system architecture that can be tailored to the needs of the embedded system designer.TRUE
30. Managers are users of domains that must observe the access permissions of the individual sections and/or pages that make up that domain.FALSE

**CHAPTER 11**

1. The operand \_\_\_\_\_\_\_\_ yields true if and only if both of its operands are true.  
   a. XOR  
   b. OR  
   c. AND  
   d. NOT
2. The operation \_\_\_\_\_\_\_\_\_ yields true if either or both of its operands are true.  
   a. NOT  
   b. AND  
   c. NAND  
   d. OR
3. The unary operation \_\_\_\_\_\_\_\_\_ inverts the value of its operand.  
   a. OR  
   b. NOT  
   c. NAND  
   d. XOR
4. A \_\_\_\_\_\_\_ is an electronic circuit that produces an output signal that is a simple Boolean operation on its input signals.  
   a. gate  
   b. decoder  
   c. counter  
   d. flip-flop
5. Which of the following is a functionally complete set?  
   a. AND, NOT  
   b. NOR  
   c. AND, OR, NOT  
   d. all of the above
6. For more than four variables an alternative approach is a tabular technique referred to as the \_\_\_\_\_\_\_\_\_ method.  
   a. DeMorgan  
   b. Quine-McCluskey  
   c. Karnaugh map  
   d. Boole-Shannon
7. \_\_\_\_\_\_\_\_ are used in digital circuits to control signal and data routing.  
   a. Multiplexers  
   b. Program counters  
   c. Flip-flops  
   d. Gates
8. \_\_\_\_\_\_\_\_ is implemented with combinational circuits.  
   a. Nano memory  
   b. Random access memory  
   c. Read only memory  
   d. No memory
9. The \_\_\_\_\_\_\_\_ exists in one of two states and, in the absence of input, remains in that state.  
   a. assert  
   b. complex PLD  
   c. decoder  
   d. flip-flop
10. The \_\_\_\_\_\_\_\_ flip-flop has two inputs and all possible combinations of input values are valid.  
    a. J-K  
    b. D  
    c. S-R  
    d. clocked S-R
11. A \_\_\_\_\_\_\_\_\_ accepts and/or transfers information serially.  
    a. S-R latch  
    b. shift register  
    c. FPGA  
    d. parallel register
12. Counters can be designated as \_\_\_\_\_\_\_\_\_.  
    a. asynchronous  
    b. synchronous  
    c. both asynchronous and synchronous  
    d. neither asynchronous or synchronous
13. CPUs make use of \_\_\_\_\_\_\_\_\_ counters, in which all of the flip-flops of the counter change at the same time.  
    a. synchronous  
    b. asynchronous  
    c. clocked S-R  
    d. timed ripple
14. The \_\_\_\_\_\_\_\_\_ table provides the value of the next output when the inputs and the present output are known, which is exactly the information needed to design the counter or any sequential circuit.  
    a. excitation  
    b. Kenough  
    c. J-K flip-flop  
    d. FPGA
15. A \_\_\_\_\_\_\_\_\_ is a PLD featuring a general structure that allows very high logic capacity and offers more narrow logic resources and a higher ration of flip-flops to logic resources than do CPLDs.  
    a. SPLD  
    b. FPGA  
    c. PAL  
    d. PLA
16. The operation of the digital computer is based on the storage and processing of binary data. TRUE
17. Claude Shannon, a research assistant in the Electrical Engineering Department at M.I.T., proposed the basic principles of Boolean algebra. FALSE
18. In the absence of parentheses, the AND operation takes precedence over the OR operation. TRUE
19. Logical functions are implemented by the interconnection of decoders. FALSE
20. The delay by the propagation time of signals through the gate is known as the gate delay. TRUE
21. A combinational circuit consists of n binary inputs and m binary outputs. TRUE
22. Any Boolean function can be implemented in electronic form as a network of gates. TRUE
23. A Boolean function can be realized in the sum of products (SOP) form but not in the product of sums (POS) form. FALSE
24. "Don't care" conditions are when certain combinations of values of variables never occur, and therefore the corresponding output never occurs. TRUE
25. The value to be loaded into the program counter can come from a binary counter, the instruction register, or the output of the ALU.TRUE
26. In general, a decoder has n inputs and 2n outputs.TRUE
27. Combinational circuits are often referred to as "memoryless" circuits because their output depends only on their current input and no history of prior inputs is retained.TRUE
28. Binary addition is exactly the same as Boolean algebra.FALSE
29. Events in the digital computer are synchronized to a clock pulse so that changes occur only when a clock pulse occurs. TRUE
30. A register is a digital circuit used within the CPU to store one or more bits of data.TRUE

**CHAPTER 13**

1. The advantage of \_\_\_\_\_\_\_\_\_\_ is that no memory reference other than the instruction fetch is required to obtain the operand.  
   a. direct addressing  
   b. immediate addressing  
   c. register addressing  
   d. stack addressing
2. The principal advantage of \_\_\_\_\_\_\_\_\_\_\_ addressing is that it is a very simple form of addressing.  
   a. displacement  
   b. register  
   c. stack  
   d. direct
3. \_\_\_\_\_\_\_\_\_\_ has the advantage of large address space, however it has the disadvantage of multiple memory references.  
   a. Indirect addressing  
   b. Direct addressing  
   c. Immediate addressing  
   d. Stack addressing
4. The advantages of \_\_\_\_\_\_\_\_\_ addressing are that only a small address field is needed in the instruction and no time-consuming memory references are required.  
   a. direct  
   b. indirect  
   c. register  
   d. displacement
5. \_\_\_\_\_\_\_\_\_\_ has the advantage of flexibility, but the disadvantage of complexity.  
   a. Stack addressing  
   b. Displacement addressing  
   c. Direct addressing  
   d. Register addressing
6. For \_\_\_\_\_\_\_\_\_, the address field references a main memory address and the referenced register contains a positive displacement from that address.  
   a. indexing  
   b. base-register addressing  
   c. relative addressing  
   d. all of the above
7. Indexing performed after the indirection is \_\_\_\_\_\_\_\_\_\_.  
     
   a. relative addressing  
   b. autoindexing  
   c. postindexing  
   d. preindexing
8. For the \_\_\_\_\_\_\_\_\_ mode, the operand is included in the instruction.  
   a. immediate  
   b. base  
   c. register  
   d. displacement
9. The only form of addressing for branch instructions is \_\_\_\_\_\_\_\_\_ addressing.  
   a. register  
   b. relative  
   c. base  
   d. immediate
10. Which of the following interrelated factors go into determining the use of the addressing bits?  
    a. number of operands  
    b. number of register sets  
    c. address range  
    d. all of the above
11. \_\_\_\_\_\_\_\_\_ is a principle by which two variables are independent of each other.  
    a. Opcode  
    b. Orthogonality  
    c. Completeness  
    d. Autoindexing
12. The \_\_\_\_\_\_\_\_\_ was designed to provide a powerful and flexible instruction set within the constraints of a 16-bit minicomputer.  
    a. PDP-1  
    b. PDP-8  
    c. PDP-11  
    d. PDP-10
13. The \_\_\_\_\_\_\_\_\_\_ byte consists of three fields: the Scale field, the Index field and the Base field.  
    a. SIB  
    b. VAX  
    c. PDP-11  
    d. ModR/M
14. All instructions in the ARM architecture are \_\_\_\_\_\_\_\_\_\_ bits long and follow a regular format.  
    a. 8  
    b. 16  
    c. 32  
    d. 64
15. \_\_\_\_\_\_\_\_\_\_ is a design principle employed in designing the PDP-10 instruction set.  
    a. Orthogonality  
    b. Completeness  
    c. Direct addressing  
    d. All of the above
16. The value of the mode field determines which addressing mode is to be used.TRUE
17. In a system without virtual memory, the effective address is a virtual address or a register. FALSE
18. The disadvantage of immediate addressing is that the size of the number is restricted to the size of the address field. TRUE
19. With direct addressing, the length of the address field is usually less than the word length, thus limiting the address range. TRUE
20. Register addressing is similar to direct addressing with the only difference being that the address field refers to a register rather than a main memory address. TRUE
21. Register indirect addressing uses the same number of memory references as indirect addressing. FALSE
22. Three of the most common uses of stack addressing are relative addressing, base-register addressing, and indexing.FALSE
23. The method of calculating the EA is the same for both base-register addressing and indexing.TRUE
24. Typically an instruction set will include both preindexing and postindexing.FALSE
25. The x86 is equipped with a variety of addressing modes intended to allow the efficient execution of high-level languages.TRUE
26. The base with index and displacement mode sums the contents of the base register, the index register, and a displacement to form the effective address. TRUE
27. The memory transfer rate has not kept up with increases in processor speed.TRUE
28. For addresses that reference memory the range of addresses that can be referenced is not related to the number of address bits.FALSE
29. The principal price to pay for variable-length instructions is an increase in the complexity of the processor. TRUE
30. One advantage of linking the addressing mode to the operand rather than the opcode is that any addressing mode can be used with any opcode. TRUE

**CHAPTER 14**

1. \_\_\_\_\_\_\_\_\_\_ are a set of storage locations.  
   a. Processors  
   b. PSWs  
   c. Registers  
   d. Control units
2. The \_\_\_\_\_\_\_\_ controls the movement of data and instructions into and out of the processor.  
   a. control unit  
   b. ALU  
   c. shifter  
   d. branch
3. \_\_\_\_\_\_\_\_ registers may be used only to hold data and cannot be employed in the calculation of an operand address.  
   a. General purpose  
   b. Data  
   c. Address  
   d. Condition code
4. \_\_\_\_\_\_\_\_\_\_ are bits set by the processor hardware as the result of operations.  
   a. MIPS  
   b. Condition codes  
   c. Stacks  
   d. PSWs
5. The \_\_\_\_\_\_\_\_\_ contains the address of an instruction to be fetched.  
   a. instruction register  
   b. memory address register  
   c. memory buffer register  
   d. program counter
6. The \_\_\_\_\_\_\_\_ determines the opcode and the operand specifiers.  
   a. decode instruction  
   b. fetch operands  
   c. calculate operands  
   d. execute instruction
7. \_\_\_\_\_\_\_\_\_ is a pipeline hazard.  
   a. Control  
   b. Resource  
   c. Data  
   d. All of the above
8. A \_\_\_\_\_\_\_\_ hazard occurs when there is a conflict in the access of an operand location.  
   a. resource  
   b. data  
   c. structural  
   d. control
9. A \_\_\_\_\_\_\_\_\_ is a small, very-high-speed memory maintained by the instruction fetch stage of the pipeline and containing the n most recently fetched instructions in sequence.  
   a. loop buffer  
   b. delayed branch  
   c. multiple stream  
   d. branch prediction
10. The \_\_\_\_\_\_\_\_\_ is a small cache memory associated with the instruction fetch stage of the pipeline.  
    a. dynamic branch  
    b. loop table  
    c. branch history table  
    d. flag
11. The \_\_\_\_\_\_\_\_\_ stage includes ALU operations, cache access, and register update.  
    a. decode  
    b. execute  
    c. fetch  
    d. write back
12. \_\_\_\_\_\_\_\_ is used for debugging.  
    a. Direction flag  
    b. Alignment check  
    c. Trap flag  
    d. Identification flag
13. The ARM architecture supports \_\_\_\_\_\_\_ execution modes.  
    a. 2  
    b. 8  
    c. 11  
    d. 7
14. The OS usually runs in \_\_\_\_\_\_\_\_.  
    a. supervisor mode  
    b. abort mode  
    c. undefined mode  
    d. fast interrupt mode
15. The \_\_\_\_\_\_\_\_\_ contains a word of data to be written to memory or the word most recently read.  
    a. MAR  
    b. PC  
    c. MBR  
    d. IR
16. The processor needs to store instructions and data temporarily while an instruction is being executed. TRUE
17. The control unit (CU) does the actual computation or processing of data. FALSE
18. Within the processor there is a set of registers that function as a level of memory above main memory and cache in the hierarchy. TRUE
19. Condition codes facilitate multiway branches.TRUE
20. The allocation of control information between registers and memory are not considered to be a key design issue. FALSE
21. Instruction pipelining is a powerful technique for enhancing performance but requires careful design to achieve optimum results with reasonable complexity. TRUE
22. The cycle time of an instruction pipeline is the time needed to advance a set of instructions one stage through the pipeline. TRUE
23. A control hazard occurs when two or more instructions that are already in the pipeline need the same resource. FALSE
24. One of the major problems in designing an instruction pipeline is assuring a steady flow of instructions to the initial stages of the pipeline. TRUE
25. The predict-never-taken approach is the most popular of all the branch prediction methods. TRUE
26. It is possible to improve pipeline performance by automatically rearranging instructions within a program so that branch instructions occur later than actually desired. TRUE
27. Interrupt processing allows an application program to be suspended in order that a variety of interrupt conditions can be serviced and later resumed. TRUE
28. An interrupt is generated from software and it is provoked by the execution of an instruction. FALSE
29. While the processor is in user mode the program being executed is unable to access protected system resources or to change mode, other than by causing an exception to occur. TRUE
30. The exception modes have full access to system resources and can change modes freely. TRUE

**CHAPTER 15**

1. \_\_\_\_\_\_\_\_\_ determines the control and pipeline organization.  
   a. Calculation  
   b. Execution sequencing  
   c. Operations performed  
   d. Operands used
2. The Patterson study examined the dynamic behavior of \_\_\_\_\_\_\_\_\_ programs, independent of the underlying architecture.  
   a. HLL  
   b. RISC  
   c. CISC  
   d. all of the above
3. \_\_\_\_\_\_\_\_ is the fastest available storage device.  
   a. Main memory  
   b. Cache  
   c. Register storage  
   d. HLL
4. The first commercial RISC product was \_\_\_\_\_\_\_\_\_.  
   a. SPARC  
   b. CISC  
   c. VAX  
   d. the Pyramid
5. \_\_\_\_\_\_\_\_\_ instructions are used to position quantities in registers temporarily for computational operations.  
   a. Load-and-store  
   b. Window  
   c. Complex  
   d. Branch
6. Which stage is required for load and store operations?  
   a. I  
   b. E  
   c. D  
   d. all of the above
7. The instruction location immediately following the delayed branch is referred to as the \_\_\_\_\_\_\_\_.  
   a. delay load  
   b. delay file  
   c. delay slot  
   d. delay register
8. A \_\_\_\_\_\_\_\_ instruction can be used to account for data and branch delays.  
   a. SUB  
   b. NOOP  
   c. JUMP  
   d. all of the above
9. A tactic similar to the delayed branch is the \_\_\_\_\_\_\_\_\_, which can be used on LOAD instructions.  
   a. delayed load  
   b. delayed program  
   c. delayed slot  
   d. delayed register
10. The MIPS R4000 uses \_\_\_\_\_\_\_\_ bits for all internal and external data paths and for addresses, registers, and the ALU.  
    a. 16  
    b. 32  
    c. 64  
    d. 128
11. All MIPS R series processor instructions are encoded in a single \_\_\_\_\_\_\_\_ word format.  
    a. 4-bit  
    b. 8-bit  
    c. 16-bit  
    d. 32-bit
12. A \_\_\_\_\_\_\_\_\_ architecture is one that makes use of more, and more fine-grained pipeline stages.  
    a. parallel  
    b. superpipelined  
    c. superscalar  
    d. hybrid
13. The R4000 can have as many as \_\_\_\_\_\_\_ instructions in the pipeline at the same time.  
    a. 8  
    b. 10  
    c. 5  
    d. 3
14. SPARC refers to an architecture defined by \_\_\_\_\_\_\_\_.  
    a. Microsoft  
    b. Apple  
    c. Sun Microsystems  
    d. IBM
15. The R4000 pipeline stage where the instruction result is written back to the register file is the \_\_\_\_\_\_\_\_\_\_ stage.  
    a. write back  
    b. tag check  
    c. data cache  
    d. instruction execute
16. Microprogramming eases the task of designing and implementing the control unit and provides support for the family concept. TRUE
17. Pipelining is a means of introducing parallelism into the essentially sequential nature of a machine-instruction program. TRUE
18. The major cost in the life cycle of a system is hardware. FALSE
19. It is common for programs, both system and application, to continue to exhibit new bugs after years of operation. TRUE
20. Procedure calls and returns are not important aspects of HLL programs. FALSE
21. The register file is on the same chip as the ALU and control unit. TRUE
22. The register file employs much shorter addresses than addresses for cache and memory. TRUE
23. To handle any possible pattern of calls and returns the number of register windows would have to be unbounded. TRUE
24. Cache memory is a much faster memory than the register file. FALSE
25. The cache is capable of handling global as well as local variables. TRUE
26. When using graph coloring, nodes that share the same color cannot be assigned to the same register. FALSE
27. With simple, one cycle instructions, there is little or no need for microcode. TRUE
28. Almost all RISC instructions use simple register addressing. TRUE
29. RISC processors are more responsive to interrupts because interrupts are checked between rather elementary operations. TRUE
30. Unrolling can improve performance by increasing instruction parallelism by improving pipeline performance. TRUE

MORE QUESTIONS

1. The routine executed in response to an interrupt request is called **interrupt service (ISR)** routine.
2. The correspondence between the main memory blocks and those in the cache is specified by a **mapping function**
3. What is stored in the stack pointer? **Address of top item.**
4. Cycle stealing is used in **DMA**
5. Assume an instruction set that uses a fixed 14-bit instruction length. Operand specifiers are 8 bits in length. What is the maximum number of one operand instructions that can be supported? **2^6 = 64.**
6. Assembly: INT 21h/ AH = 1 is **read character from standard input, result is stored in AL**
7. Techniques that automatically move program and data blocks into the physical main memory when they are required for execution are called **virtual-memory techniques.**
8. Consider a magnetic disk drive with 4 surfaces, 512 tracks per surface, and 32 sectors per track, sector size is 512 byte. What is the disk capacity? **32MB.**
9. The performance of the cache memory is measured in terms of a quantity called **hit ratio**
10. The **PC** holds the address of the next instruction to be fetched.
11. The **IR** holds last instruction fetched.
12. The **fetch** cycle occurs at the beginning of each instruction cycle an causes an instruction to be fetched from memory.
13. Which of the following is an example of sequential access media? **Magnetic tapes.**
14. What is the purpose of RAID systems? **It increases the disk storage capacity and availability**
15. The **MAR** is connected to the address lines of the system bus.
16. The **MAR** holds the address of the storage location being accessed from memory.
17. Instruction register stores **instruction which is currently executed**
18. A computer has 256k words, how many bits are required to specify the address part? **18**